SPECIFICATION

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[CONTACTLESS CHANNEL WRITE/ERASE FLASH MEMORY CELL AND ITS FABRICATION METHOD]

Cross Reference To Related Applications

This application is a division of application Serial No. 09/683,581 filed on 01/22/2002.

Background of Invention

[0001] 1.Field of the Invention

[0002] The present invention relates tothe field of non-volatile memorys, and more particularly, to a contactless channel write/erase flash memory cell/array and method of fabricating the same.

[0003] 2.Description of the Prior Art

[0004] Fig.1 is a cross-sectional view illustrating a conventional flash memory cell 10. Fig.2 is a cross-section view illustrating a metal contact structure associated with the conventional flash memory cell structure. Referring to Fig.1, the flash memory cell 10 is built upon a P-substrate 11 including a N-well 12 formed on the P-substrate 11 and a stacked gate 14 formed on the N-well 12. An N^+-doped region 16 and an N^+-doped region 18, functioning as a source and a drain of the flash memory cell 10, respectively, are formed two sides of the stacked gate 14 in the N-well 12 respectively. A P-doped region 20 is formed surrounding the N^+-doped region 18 in the N-well 12 and a P-doped region 22 is formed beneath the stacked gate 14.

[0005] The stacked gate 14 includes a control gate 24 and a floating gate 26. A word line voltage V_{WL} is applied to the control gate 24 for controlling the flash memory cell 10. The floating gate 26 is in a "floating" state without any direct connection with external circuits for storing charges. A source voltage V_{SL} is applied to the N^+-doped region 16 (source terminal), and a drain voltage V_{BL} is applied to the N^+-doped region 18 (drain terminal).

[0006] With these applied voltages, electrons (e^-) eject from the floating gate 26 to the N^+-doped region 18 due to the edge Fowler-Nordheim effect and the flash memory cell 10 is programmed. However, upon applying a voltage on the drain terminal, an undesirable depletion region outside the N^+-doped region 18 is also produced. Furthermore, hot holes (e^+) will be generated leading to hot hole injection in the presence of lateral electric field. These hot holes can severely affect the normal operation of a flash memory cell 10. With a short-circuiting connection between the N^+-doped region 18 of the drain terminal and the P-doped region 20, the above-mentioned problems can be prevented. Referring to Fig.2, a metal contact 30 penetrates through an N^+-doped region 32 of each drain terminal and into a P-doped region 34. A bit line voltage V_{BL} is applied to the N^+-doped region 32 of each drain terminal through the metal contact 30 so that the N^+-doped region 32 and the P-doped region 34 are short-circuited together.

[0007] In addition, a predetermined distance 38 between the metal contact 30 and the stacked gate 36 has to be maintained in the conventional flash memory cell for preventing interferences caused by each other. However, increasing cell density is constantly in demand in current market, and such conventional flash memory cell design apparently can not satisfy such demand.

Summary of Invention

[0008] It is therefore a primary objective of the present invention to provide a contactless channel write/erase flash memory cell by varying a connecting mode of a metal contact to increase memory packing density without affectingthe source of a neighboring flash memory cell.

[0009] It is another object of the present invention to provide a method of fabricating a

contactless channel write/erase flash memory cell.

[0010] According to the claimed invention, a flash memory array includes a plurality of contactless channel write/erase flash memory cells, and each memory cell includes a multi-level substrate, a first ion doped region, a floating gate, a tunnel oxide layer, a second ion doped region, a third ion doped region, a fourth ion doped region, two isolating oxide layers, a dielectric layer and a control gate. The tunnel oxide is located on the substrate, and the floating gate is located on the tunnel oxide layer, the first ion doped region acting as a drain is located on one side of the floating gate of the substrate, the second ion doped region is located surrounding a bottom of the first ion doped region, the third ion doped region is located beneath the floating gate with one side bordering on the second ion doped region, the fourth ion doped region that acts as a source is located in the substrate with one side bordering on the third ion doped region, the two isolating oxide layers are located on the first ion doped region and the fourth ion doped region respectively, the dielectric layer is located on the floating gate and the two isolating oxide layers, and the control gate is located above the floating gate and the two isolating oxide layers.

[0011] According to the present invention, the control gate of the flash memory cell extends laterally in a word line direction, and the first ion doped region and the second ion doped region extend in a bit line direction. Therefore, a metal contact which a bit line voltage applied to can be designed away from any of the first ion doped region and the second ion doped region of the memory cells in a bit line direction to decrease the number of the metal contact and also to reduce the area of the memory array.

[0012] The substrate, from bottom to top, includes a N-substrate, a deep P-well and a N-well. The first ion doped region and the fourth ion doped region are N^+-doped region formed by implanting phosphorous (P) or arsenic (As) ions, the second ion doped region and the third ion doped region are P-doped region formed by implanting boron (B) ions, and the second ion doped region has a depth much greater than the third ion doped region.

[0013] In addition, the first ion doped region and the second ion doped region are short-circuiting together, such as using a metal contact penetrating through junction

between the first ion doped region and the second ion doped region, or using a metal contact crossing the exposed first ion doped region and the exposed second ion doped region.

[0014] Furthermore, the present invention further provides a fabricating method of a contactless channel write/erase flash memory cell. The flash memory cell is formed on a substrate. First, a shallow P-doped region is formed within the substrate, and then a tunnel oxide layer and a floating gate are formed on the shallow P-doped region, respectively. Next, a deep P-doped region is formed one side of the floating gate in the substrate, and two N^+ -doped regions are formed on the deep P-doped region and another side of the floating gate within the substrate respectively. Two isolating oxide layers are formed on the two N^+ -doped regions, and a dielectric layer is formed on the floating gate and the two N^+ -doped regions. Finally, a control gate is formed on the dielectric layer.

[0015] The substrate includes a N-substrate, a deep P-well region and a N-well region. The N-substrate is formed first, and then the deep P-well region is formed on the N-substrate. Finally, an N-well region is formed on the deep P-well region.

[0016] At least one bit line metal contact is formed outside the block of the flash memory array. The metal contact penetrates through the isolating oxide layer and the junction between the N^+ -doped region and the deep P-doped region. In an alternative method, the metal contact crosses the exposed N^+ -doped region and the exposed deep P-doped region which short-circuits these two regions.

[0017] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0018] Fig.1 is a cross-section view illustrating a conventional flash memory cell structure.

[0019] Fig.2 is a cross-section view illustrating a metal contact structure associated with the conventional flash memory cell structure.

[0020] Fig.3 is a cross-section view illustrating a write/erase flash memory cell structure according to the first embodiment of the present invention.

[0021] Fig.4A is a cross-section view of the flash memory cell structure shown in Fig.4B and Fig.4B is a top view of the write/erase flash memory cell structure according to the first embodiment of the present invention.

[0022] Fig.5A is a cross-sectional view illustrating one type of metal contact structure associated with the write/erase flash memory cell structure according to the first embodiment of the present invention.

[0023] Fig.5Bis a cross-sectional view illustrating another type of metal contact structure associated with the write/erase flash memory cell structure according to the first embodiment of the present invention.

[0024] Fig.6 is a cross-section view illustrating another write/erase flash memory cell structure according to the second embodiment of the present invention.

[0025] Fig.7A through Fig.7E are cross-section views illustrating the fabrication process of the write/erase flash memory cell structure according to the first embodiment of the present invention.

[0026] Fig.8A through Fig.8C are three circuit diagrams illustrating various modes of operation of write/erase flash memory cell structure according to the first embodiment of the present invention.

Detailed Description

[0027] Referring to Fig.3, Fig.3 is a cross-sectional view illustrating a contactless channel write/erase flash memory cell according to the present invention. A flash memory array (not shown) is installed in a semiconductor wafer (not shown) having a plurality of flash memory cells arranged along a line direction. The line direction is a bit line direction or a word line direction perpendicularly to the bit line direction. Each cell includes a multi-level substrate 100, a first ion doped region 102, a tunnel oxide layer 103,a floating gate 104, a second ion doped region 106, a third ion doped region 108, a fourth ion doped region 110, two isolating oxide layers 112 and 114,a dielectric layer 116 and a control gate 118.

[0028] The multi-level substrate 100, from bottom to top, includes an N-substrate 120, a deep P-well 122 and an N-well 124. The first ion doped region 102, functioning as a drain, is formed by implanting N^+-type ions into the N-well 124 of the substrate 100. The tunnel oxide layer 103 locates between the floating gate 104 and the N-well 124 of the substrate 100, and the floating gate 104 locates on the tunnel oxide layer 103 next to the first ion doped region 102. The second ion doped region 106 is formed by implanting P-type ions into a bottom of the first ion doped region 102 and locates on the surrounding area of the first ion doped region 102. The third ion doped region 108 is formed by implanting P-ions into the N-well 124 and locates beneath the floating gate 104, with one side connected to the second ion doped region 106. The second ion doped region 106 has a depth much greater than the third ion doped region 108. The fourth ion doped region 110, that acts as a source of the flash memory cell, locates within the N-well 124 of the substrate 100, with one side connected to the third ion doped region 108. The two isolating oxide layers 112 and 114 locate on the first ion doped region 102 and the fourth ion doped region 110 respectively. The dielectric layer 116 locates on the floating gate 104 and the two isolating oxide layers 112 and 114, and the control gate 118 locates above the floating gate 104 and the two isolating layers 112 and 114.

[0029] Referring to Fig.4A and Fig.4B,Fig.4B is a top view of a contactless write/erase flash memory array according to the first embodiment of the present invention and Fig.4A is a cross-section view of the flash memory array shown in Fig.4B. The control gates 118, 140 extend to the word line direction and a word line voltage is applied to the control gate 118. The first ion doped region 102 and the second ion doped region 106 extend along the bit line direction, and adjacent first ion doped regions and adjacent second ion doped regions are connected with each other, respectively. A bit line voltage is applied to the first ion doped region 102 and the second ion doped region 106. The first ion doped region 102 and the second ion doped region106 are connected through only one metal contact (not shown), and the metal contact is installed in a via hole 146, shown in Fig.4B, penetrating through junction between the first ion doped region 102 and the second ion doped region 106. The control gate 118 locates between the two field oxide layers 130 and 132, and the control gate 118 stretches over a plurality of floating gates, such as the floating gates 134 and 136.

Furthermore, an overlapped portion 138 of the first ion doped region 102 and the second ion doped region 106 located one side of the floating gate 134 and beneath the control gate 118 extends along the bit line direction. Therefore, the bit line voltage is applied to the via hole 146 through the metal contact, and the metal contact is installed away from any of the first ion doped region 102 and the second ion doped region 106 of the memory cells to avoid electrical interference between the metal contact and the floating gate 118 of each of the memory cells.

[0030] In addition, the first ion doped region 102 and the second ion doped region 106 are short-circuited together using a metal contact 148. Referring to Fig.5A, Fig.5A is a cross-sectional view illustrating metal contact structure associated withthe write/erase flash memory cell structure according to the first embodiment of the present invention. The metal contact 148 penetrates through first ion doped region 150 and into second ion doped region 152 so that the two regions are short-circuited together. Referring to Fig.5B, Fig.5Bis a cross-sectional view illustrating another type of metal contact structure associated with the write/erase flash memory cell structure according to the present invention. Metal contact 148 is formed across the exposed first ion doped region 150 and the exposed second ion doped region 152 and thus short-circuits the two regions together.

[0031] Fig.6 is a cross-section view illustrating another contactless write/erase flash memory cell structure according to the second embodiment of the present invention. In this embodiment, the floating gate 104 shown in Fig.3 is changed to a first floating gate 105 and a second floating gate 107. The first floating gate 105 locates on the third ion doped region 108 between the two isolating oxide layers 112 and 114, and the second floating gate 107 locates on the first floating gate 105 and a portion of the two isolating oxide layers 114 and 114. The first floating gate 105 and the second floating gate 107 are short-circuited. Since the overlapped area between the second floating gate 107 and the control gate is increased, the capacitance coupling effect is enhanced which increases the operating efficiency of the flash memory cell.

[0032]

Furthermore, the present invention provides a fabricating method of a contactless channel write/erase flash memory cell. Fig.7A through Fig.7E are cross-section views illustrating the fabrication process of the write/erase flash memory cell structure

according to the first embodiment of the present invention. Referring to Fig.7A, a multi-level substrate 200, from bottom to top, including an N-substrate 208, a deep P-well 206 and an N-well 204, is formed. A shallow trench isolation (STI) or a field oxide layer (not shown) is formed on two sides of the substrate 200. And a P-doped region 202 is formed within the substrate 200 by implanting P-type ions into the substrate 200. Referring to Fig.7B, a tunnel oxide layer 210 is formed on the substrate 200, and a first polysilicon layer 212 that acts as a floating gate and a silicon nitride layer 214 are deposited on the tunnel oxide layer 210. And a photolithographic and etching process is performed to form the structure shown in Fig.7B.

[0033] Referring to Fig.7C, a P-doped region 216 is formed on one side of the first polysilicon layer 212 within the N-well 204 by using a P-type ion mask and P-type ions of fluoride boron (BF_2) into the N-well 204 of the substrate 200. And an N^+-doped region 218 and an N^+-doped region 220 are formed on the P-doped region 216 and another side of the first polysilicon layer 212 within the N-well 204 by implanting N^+-type ions, such as arsenic (As) into the N-well 204 of the substrate 200. Referring to Fig.7D, two isolating oxide layers 222 and 224 are formed on the N^+-doped region 218 and the N^+-doped region 220, and the silicon nitride layer 214 on the first polysilicon layer 212 is removed. Finally referring to Fig.7E, a dielectric layer 226 is deposited on the first polysilicon layer 212 and the two isolating oxide layers 222 and 224, and a second polysilicon layer 228 is deposited on the dielectric layer 226. Further, a stacked gate etching process is performed to remove portions of the first polysilicon layer 212 and the second polysilicon layer 228, and the second polysilicon layer 228 that acts as a word line is a long strip. Thereafter, a via hole is formed away from any of the N^+-doped region and the P-doped region of the flash memory cell as shown in Fig.4B, and a bit line metal contact penetrates through the isolating oxide layers 222 and 224, and junction between the N^+-doped region 218 and the P-doped region 216, thereby short-circuiting the N^+-doped region 218 and into the P-doped region 216together.

[0034] The operating method for operating the contact channel write/erase flash memory cell will be introduced below.

[0035] Fig.8A through Fig.8C are three circuit diagrams illustrating various modes of

operations of the write/erase flash memory cell structure according to the first embodiment of the present invention. Referring to Fig.8A through Fig.8C, the Fowler-Nordheim tunneling effect is induced to program or erase the flash memory cell. A word line voltage V_{WL}, a source line voltage V_{SL} and a bit line voltage V_{BL} are applied to a control gate, a source terminal and a drain terminal of the flash memory cell 300 respectively. A P-doped region of the flash memory cell 300 and the bit line voltage are short-circuited together.

[0036] Referring to Fig.8A, during an erasing operation of the flash memory cell 300, a high voltage is applied to the word line, such as V_{WL} = 18 to 10 Volts, and a voltage lower than the word line voltage is applied to the source terminal, such as V_{SL} =0 to -8 Volts. Voltage of the bit line remains in afloating state. With such configuration, electrons of the source terminal are injected into the floating gate of the flash memory cell 300, thereby increasing a threshold voltage of the flash memory cell and achieving the necessary data-erase operation.

[0037] Referring to Fig.8B, during a programming operation of the flash memory cell a low voltage is applied to the word line, such as V_{WL} = -12 to -8 Volts, and a voltage higher than the word line voltage is applied to the bit line, such as V_{BL} =6 to 9 Volts. Voltage of the source terminal V_{SL} remains in afloating state. With such configuration, trapped floating gate electrons are injected away through a channel of the flash memory cell 300, thereby decreasing a threshold voltage of the flash memory cell and achieving the necessary programming operation.

[0038] Referring to Fig.8C, during a reading data operation of the flash memory cell 300, a voltage is applied to the word line, such as V_{WL} = 2 to 5 Volts, a voltage lower than the word line voltage is applied to the source terminal, such as V_{SL} =0 to 2 Volts, and a voltage lower than the source terminal is applied to the bit line, such as V_{SL} =-2 to 0 Volts. With such configuration, stored data can be read from the flash memory cell 300.

[0039] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.